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(1014311) : 1014311 : Digital Marketing
(2324111) : 2324111 : Mathematics-IV
(2324114) : 2324114 : Electronic circuits & Design lab
(2994511) : 2994511 : Business Model Development
(2114211) : 2114211 : Computer Organization & Architecture
(2324112) : 2324112 : Electronic circuits & Design
(2324115) : 2324115 : Physics of Semiconductor devices Lab
(2994512) : 2994512 : Design Thinking
(2114212) : 2114212 : Computer Organization & Architecture Lab
(2324113) : 2324113 : Physics of Semiconductor devices
(2324413) : 2324413 : Creative Coding in Python

Course Code	Course Title	Course Credits	I1 (INTERNAL EXAMINATION)		E1 (EXTERNAL EXAMINATION)		T1 (TERM WORK)		O1 (ORAL)		TOTALF (TOTAL MARKS)	
			Min Marks	Max Marks	Min Marks	Max Marks	Min Marks	Max Marks	Min Marks	Max Marks	Min Marks	Max Marks
1014311	Digital Marketing	2.00	8.00	20.00	12.00	30.00	...	...	...	...	20.00	50.00
2114211	Computer Organization & Architecture	3.00	16.00	40.00	24.00	60.00	...	...	...	...	40.00	100.00
2114212	Computer Organization & Architecture Lab	1.00	...	...	...	...	10.00	25.00	10.00	25.00	20.00	50.00
2324111	Mathematics-IV	3.00	16.00	40.00	24.00	60.00	10.00	25.00	...	...	50.00	125.00
2324112	Electronic circuits & Design	3.00	16.00	40.00	24.00	60.00	...	...	...	...	40.00	100.00
2324113	Physics of Semiconductor devices	3.00	16.00	40.00	24.00	60.00	...	...	...	...	40.00	100.00
2324114	Electronic circuits & Design lab	1.00	...	...	...	...	10.00	25.00	10.00	25.00	20.00	50.00
2324115	Physics of Semiconductor devices Lab	1.00	...	...	...	...	10.00	25.00	10.00	25.00	20.00	50.00
2324413	Creative Coding in Python	2.00	...	...	...	...	20.00	50.00	10.00	25.00	30.00	75.00
2994511	Business Model Development	2.00	...	...	...	...	20.00	50.00	...	...	20.00	50.00
2994512	Design Thinking	2.00	...	...	...	...	20.00	50.00	...	...	20.00	50.00

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)			
		TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)				TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)			
External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
132410001	AARYA AMIT JOSHI		Regular	MALE	(MU0341120252004712)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1		18 P	17 P				16 P	13 P	42 P	37 P	35 P			
O1		20 P					19 P	14 P	22 P					
E1 27 P	34 P		19 *5 P		24 P	36 P						MARKS		
I1 14 P	28 P		22 P		16 P	16 P						(494)		PASS
TOT 41 9 A+ 2 18.0	62 7 B+ 3 21.0	38 8 A 1 8.0	63 5 C 3 15.0		40 4 D 3 12.0	52 5 C 3 15.0	35 8 A 1 8.0	27 5 C 1 5.0	64 9 A+ 2 18.0	37 8 A 2 16.0	35 8 A 2 16.0	23	152.0	6.60870

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO: 132410002 | NAME: AELA JAGDISH APPARAO | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240217761) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

Course	Scheme	T1	O1	E1	I1	TOT	GP	G	C	G*C
1014311 Digital Marketing (THEORY)	External (30/12), Internal(20/8)			19 P	9 P	28	6	B	2	12.0
2114211 Computer Organization & Architecture (THEORY)	External (60/24), Internal(40/16)			24 P	17 P	41	4	D	3	12.0
2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	TERM WORK (25/10), ORAL (25/10)	15 P	18 P			33	7	B+	1	7.0
2324111 Mathematics-IV (THEORY)	TERM WORK (25/10), External (60/24), Internal(40/16)	11 P		24 P	16 P	51	4	D	3	12.0
2324112 Electronic circuits & Design (THEORY)	External (60/24), Internal(40/16)			18 *6 P	18 P	42	4	D	3	12.0
2324113 Physics of Semiconductor devices (THEORY)	External (60/24), Internal(40/16)			24 P	19 P	43	4	D	3	12.0
2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	TERM WORK (25/10), ORAL (25/10)	11 P	19 P			30	7	B+	1	7.0
2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	TERM WORK (25/10), ORAL (25/10)	15 P	14 P			29	6	B	1	6.0
2324413 Creative Coding in Python (TERM WORK AND ORAL)	TERM WORK (50/20), ORAL (25/10)	34 P	17 P			51	7	B+	2	14.0
2994511 Business Model Development (TERM WORK)	TERM WORK (50/20)	29 P				29	6	B	2	12.0
2994512 Design Thinking (TERM WORK)	TERM WORK (50/20)	28 P				28	6	B	2	12.0

TOTAL (800)	äC	RESULT äCG	REMARK äCG
MARKS (405)	23	118.0	PASS 5.13043

SEAT NO: 132410003 | NAME: AMBULKAR AARYAN VILAS | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240210528) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

Course	Scheme	T1	O1	E1	I1	TOT	GP	G	C	G*C
1014311 Digital Marketing (THEORY)	External (30/12), Internal(20/8)			29 P	16 P	45	10	O	2	20.0
2114211 Computer Organization & Architecture (THEORY)	External (60/24), Internal(40/16)			42 P	32 P	74	8	A	3	24.0
2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	TERM WORK (25/10), ORAL (25/10)	19 P	18 P			37	8	A	1	8.0
2324111 Mathematics-IV (THEORY)	TERM WORK (25/10), External (60/24), Internal(40/16)	15 P		29 P	20 P	64	5	C	3	15.0
2324112 Electronic circuits & Design (THEORY)	External (60/24), Internal(40/16)			25 P	23 P	48	4	D	3	12.0
2324113 Physics of Semiconductor devices (THEORY)	External (60/24), Internal(40/16)			44 P	22 P	66	7	B+	3	21.0
2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	TERM WORK (25/10), ORAL (25/10)	17 P	20 P			37	8	A	1	8.0
2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	TERM WORK (25/10), ORAL (25/10)	16 P	18 P			34	7	B+	1	7.0
2324413 Creative Coding in Python (TERM WORK AND ORAL)	TERM WORK (50/20), ORAL (25/10)	22 P	16 P			38	5	C	2	10.0
2994511 Business Model Development (TERM WORK)	TERM WORK (50/20)	39 P				39	8	A	2	16.0
2994512 Design Thinking (TERM WORK)	TERM WORK (50/20)	31 P				31	7	B+	2	14.0

TOTAL (800)	äC	RESULT äCG	REMARK äCG
MARKS (513)	23	155.0	PASS 6.73913

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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	SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

	SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							
	132410004	ANUSH ZINGADE		Regular	MALE	(MU0341120252004883)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			17 P	11 P			11 P	14 P	36 P	34 P	30 P			
O1			17 P				17 P	13 P	14 P					
E1	22 P	24 P		17 0 F 0.0	31 P	24 P						MARKS		
I1	12 P	17 P		16 P	9 0 F 0.0	16 P						(402)		FAILED
TOT	34 7 B+ 2 14.0	41 4 D 3 12.0	34 7 B+ 1 7.0	44 0 F 3 0.0	40 0 F 3 0.0	40 4 D 3 12.0	28 6 B 1 6.0	27 5 C 1 5.0	50 7 B+ 2 14.0	34 7 B+ 2 14.0	30 7 B+ 2 14.0	23	98.0	0.00000

	SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

	SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							
	132410005	ANWAY AMARDEEP GAJBHIYE		Regular	MALE	(MU0341120252006601)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			10 P	11 P			10 P	10 P	20 P	20 P	20 P			
O1			ABS				ABS	6 0 F 0.0	ABS					
E1	12 P	1 0 F 0.0		14 0 F 0.0	3 0 F 0.0	2 0 F 0.0						MARKS		
I1	5 0 F 0.0	4 0 F 0.0		0 F 0.0	4 0 F 0.0	3 0 F 0.0						(155)		FAILED
TOT	17 0 F 2 0.0	5 0 F 3 0.0	10 0 F 1 0.0	25 0 F 3 0.0	7 0 F 3 0.0	5 0 F 3 0.0	10 0 F 1 0.0	16 0 F 1 0.0	20 0 F 2 0.0	20 4 D 2 8.0	20 4 D 2 8.0	23	16.0	0.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE
132410006	ARZAN		Regular	MALE	(MU0341120252006204)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)			
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)	External (60/24) Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			15 P	11 P			11 P	15 P	24 P	20 P	27 P			
O1			18 P				17 P	12 P	5 0 F 0.0					
E1	13 P	25 P		25 P	25 P	29 P						MARKS		
I1	10 P	17 P		17 P	13 0 F 0.0	16 P						(365)		FAILED
TOT	23 4 D 2 8.0	42 4 D 3 12.0	33 7 B+ 1 7.0	53 4 D 3 12.0	38 0 F 3 0.0	45 4 D 3 12.0	28 6 B 1 6.0	27 5 C 1 5.0	29 0 F 2 0.0	20 4 D 2 8.0	27 5 C 2 10.0	23	80.0	0.00000

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE
132410007	ATTARDE PUSHKAR NITIN		Regular	MALE	(MU0341120240210497)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)			
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)	External (60/24) Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			18 P	19 P			17 P	18 P	34 P	40 P	31 P			
O1			19 P				20 P	18 P	19 P					
E1	26 P	44 P		34 P	34 P	24 P						MARKS		
I1	14 P	26 P		36 P	26 P	26 P						(543)		PASS
TOT	40 9 A+ 2 18.0	70 8 A 3 24.0	37 8 A 1 8.0	89 8 A 3 24.0	60 7 B+ 3 21.0	50 5 C 3 15.0	37 8 A 1 8.0	36 8 A 1 8.0	53 8 A 2 16.0	40 9 A+ 2 18.0	31 7 B+ 2 14.0	23	174.0	7.56522

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

University Of Mumbai

Sep 01, 2026
Declaration Date:Sep 01, 2026

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

PAGE : 6

SEAT NO: 132410008 | NAME: BHANDARY SHARAT KUMAR PURUSHOTTAM | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240210505) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8)	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16)	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16)	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10)	2994511 Business Model Development (TERM WORK) TERM WORK (50/20)	2994512 Design Thinking (TERM WORK) TERM WORK (50/20)	TOTAL (800) äC	RESULT äCG	REMARK äCG
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			19 P	19 P			16 P	18 P	34 P	30 P	32 P			
O1			19 P				19 P	21 P	17 P					
E1	19 P	35 P		40 P	34 P	34 P						MARKS		
I1	12 P	26 P		28 P	17 P	18 P						(507)		PASS
TOT	31 7 B+ 2 14.0	61 7 B+ 3 21.0	38 8 A 1 8.0	87 7 B+ 3 21.0	51 5 C 3 15.0	52 5 C 3 15.0	35 8 A 1 8.0	39 8 A 1 8.0	51 7 B+ 2 14.0	30 7 B+ 2 14.0	32 7 B+ 2 14.0	23	152.0	6.60870

SEAT NO: 132410009 | NAME: BHOVAD SONAL PRAKASH | STATUS: Regular | GENDER: FEMALE | ERN: (MU0341120240210511) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8)	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16)	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16)	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10)	2994511 Business Model Development (TERM WORK) TERM WORK (50/20)	2994512 Design Thinking (TERM WORK) TERM WORK (50/20)	TOTAL (800) äC	RESULT äCG	REMARK äCG
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			20 P	18 P			21 P	17 P	34 P	31 P	35 P			
O1			20 P				22 P	18 P	18 P					
E1	23 P	52 P		32 P	39 P	40 P						MARKS		
I1	16 P	26 P		30 P	30 P	22 P						(564)		PASS
TOT	39 8 A 2 16.0	78 8 A 3 24.0	40 9 A+ 1 9.0	80 7 B+ 3 21.0	69 7 B+ 3 21.0	62 7 B+ 3 21.0	43 9 A+ 1 9.0	35 8 A 1 8.0	52 7 B+ 2 14.0	31 7 B+ 2 14.0	35 8 A 2 16.0	23	173.0	7.52174

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

University Of Mumbai

Sep 01, 2026
Declaration Date:Sep 01, 2026

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME		STATUS / GENDER	ERN	COLLEGE							
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)		
		ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)				
External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)							
Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)							
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		

132410010 | BILLA MADHURI MANOHAR | Regular | FEMALE | (MU0341120240210490) | MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT / REMARK
T1			15 P	15 P			18 P	13 P	30 P	32 P	32 P		
O1			18 P				20 P	17 P	19 P				
E1	26 P	30 P		33 P	48 P	44 P						MARKS	
I1	14 P	23 P		33 P	25 P	17 P						(522)	PASS
TOT	40 9 A+ 2 18.0	53 5 C 3 15.0	33 7 B+ 1 7.0	81 7 B+ 3 21.0	73 8 A 3 24.0	61 7 B+ 3 21.0	38 8 A 1 8.0	30 7 B+ 1 7.0	49 7 B+ 2 14.0	32 7 B+ 2 14.0	32 7 B+ 2 14.0	23	163.0 7.08696

SEAT NO	NAME		STATUS / GENDER	ERN	COLLEGE							
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)		
		ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)				
External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)							
Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)							
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		

132410011 | CHAVAN ANURAJ YUVRAJ | Regular | MALE | (MU0341120240210509) | MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT / REMARK
T1			16 P	15 P			18 P	17 P	32 P	34 P	31 P		
O1			18 P				18 P	17 P	17 P				
E1	27 P	29 P		27 P	25 P	31 P						MARKS	
I1	15 P	20 P		27 P	17 P	19 P						(470)	PASS
TOT	42 9 A+ 2 18.0	49 4 D 3 12.0	34 7 B+ 1 7.0	69 6 B 3 18.0	42 4 D 3 12.0	50 5 C 3 15.0	36 8 A 1 8.0	34 7 B+ 1 7.0	49 7 B+ 2 14.0	34 7 B+ 2 14.0	31 7 B+ 2 14.0	23	139.0 6.04348

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE
132410012	CHIRAYU PADYAL		Regular	MALE	(MU0341120252006480)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)				2114211 Computer Organization & Architecture (THEORY)				2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)				2324111 Mathematics-IV (THEORY)				2324112 Electronic circuits & Design (THEORY)				2324113 Physics of Semiconductor devices (THEORY)				2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)				2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)				2324413 Creative Coding in Python (TERM WORK AND ORAL)				2994511 Business Model Development (TERM WORK)				2994512 Design Thinking (TERM WORK)				TOTAL (800) äC	RESULT äCG	REMARK äCG
									TERM WORK (25/10) ORAL (25/10)				TERM WORK (25/10)												TERM WORK (25/10) ORAL (25/10)				TERM WORK (25/10) ORAL (25/10)				TERM WORK (50/20) ORAL (25/10)				TERM WORK (50/20)				TERM WORK (50/20)						
	External (30/12) Internal(20/8)				External (60/24) Internal(40/16)								External (60/24) Internal(40/16)				External (60/24) Internal(40/16)				External (60/24) Internal(40/16)																											
	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C			
T1									18	P			12	P											14	P			16	P			36	P			33	P			31	P					
O1									18	P															19	P			13	P			18	P													
E1	24	P			40	P							24	P			36	P			31	P																							MARKS		
I1	15	P			24	P							19	P			25	P			18	P																							(484)		PASS
TOT	39	8	A	2 16.0	64	7	B+	3 21.0	36	8	A	1 8.0	55	4	D	3 12.0	61	7	B+	3 21.0	49	4	D	3 12.0	33	7	B+	1 7.0	29	6	B	1 6.0	54	8	A	2 16.0	33	7	B+	2 14.0	31	7	B+	2 14.0	23	147.0	6.39130

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE
132410013	CHOUDHARY NIDHI JITENDRA		Regular	FEMALE	(MU0341120240210512)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)				2114211 Computer Organization & Architecture (THEORY)				2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)				2324111 Mathematics-IV (THEORY)				2324112 Electronic circuits & Design (THEORY)				2324113 Physics of Semiconductor devices (THEORY)				2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)				2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)				2324413 Creative Coding in Python (TERM WORK AND ORAL)				2994511 Business Model Development (TERM WORK)				2994512 Design Thinking (TERM WORK)				TOTAL (800) äC	RESULT äCG	REMARK äCG
									TERM WORK (25/10) ORAL (25/10)				TERM WORK (25/10)												TERM WORK (25/10) ORAL (25/10)				TERM WORK (25/10) ORAL (25/10)				TERM WORK (50/20) ORAL (25/10)				TERM WORK (50/20)				TERM WORK (50/20)						
	External (30/12) Internal(20/8)				External (60/24) Internal(40/16)								External (60/24) Internal(40/16)				External (60/24) Internal(40/16)				External (60/24) Internal(40/16)																											
	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C	TOT	GP	G	C G*C			
T1									22	P			20	P											20	P			18	P			36	P			34	P			33	P					
O1									20	P															22	P			22	P			16	P													
E1	18	P			48	P							42	P			49	P			45	P																							MARKS		
I1	16	P			35	P							33	P			28	P			29	P																							(606)		PASS
TOT	34	7	B+	2 14.0	83	9	A+	3 27.0	42	9	A+	1 9.0	95	8	A	3 24.0	77	8	A	3 24.0	74	8	A	3 24.0	42	9	A+	1 9.0	40	9	A+	1 9.0	52	7	B+	2 14.0	34	7	B+	2 14.0	33	7	B+	2 14.0	23	182.0	7.91304

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO | NAME | STATUS | GENDER | ERN | COLLEGE

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

132410014 | DALVI PRATISH SABAJI | Regular | MALE | (MU0341120240210531) | MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			18 P	18 P			19 P	15 P	34 P	25 P	34 P			
O1			19 P				21 P	14 P	18 P					
E1	23 P	33 P		28 P	32 P	36 P						MARKS		
I1	11 P	21 P		25 P	26 P	19 P						(489)		PASS
TOT	34 7 B+ 2 14.0	54 5 C 3 15.0	37 8 A 1 8.0	71 6 B 3 18.0	58 6 B 3 18.0	55 6 B 3 18.0	40 9 A+ 1 9.0	29 6 B 1 6.0	52 7 B+ 2 14.0	25 5 C 2 10.0	34 7 B+ 2 14.0	23	144.0	6.26087

SEAT NO | NAME | STATUS | GENDER | ERN | COLLEGE

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

132410015 | DAS BRIJBHUSHAN BIBHUTIBHUSHAN | Regular | MALE | (MU0341120240210526) | MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			12 P	13 P			18 P	14 P	30 P	25 P	30 P			
O1			17 P				18 P	23 P	16 P					
E1	21 P	27 P		14 0 F 0.0	11 0 F 0.0	19 0 F 0.0						MARKS		
I1	8 P	16 P		20 P	20 P	16 P						(388)		FAILED
TOT	29 6 B 2 12.0	43 4 D 3 12.0	29 6 B 1 6.0	47 0 F 3 0.0	31 0 F 3 0.0	35 0 F 3 0.0	36 8 A 1 8.0	37 8 A 1 8.0	46 7 B+ 2 14.0	25 5 C 2 10.0	30 7 B+ 2 14.0	23	84.0	0.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

PAGE : 10

	SEAT NO	NAME		STATUS GENDER	ERN	COLLEGE								
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
	132410016	DHAMANKAR YASHVI UMESH		Regular FEMALE	(MU0341120240210527)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1			15 P	12 P			11 P	13 P	26 P	22 P	20 P			
O1			18 P				16 P	17 P	12 P					
E1	20 P	21 0 F 0.0		29 P	24 P	19 0 F 0.0						MARKS		
I1	7 0 F 0.0	20 P		17 P	5 0 F 0.0	8 0 F 0.0						(352)		FAILED
TOT	27 0 F 2 0.0	41 0 F 3 0.0	33 7 B+ 1 7.0	58 4 D 3 12.0	29 0 F 3 0.0	27 0 F 3 0.0	27 5 C 1 5.0	30 7 B+ 1 7.0	38 5 C 2 10.0	22 4 D 2 8.0	20 4 D 2 8.0	23	57.0	0.00000

	SEAT NO	NAME		STATUS GENDER	ERN	COLLEGE								
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
	132410017	DHANSHREE CHAVAN		Regular FEMALE	(MU0341120252006710)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1			18 P	12 P			11 P	14 P	34 P	27 P	31 P			
O1			17 P				19 P	13 P	15 P					
E1	23 P	38 P		31 P	25 P	35 P						MARKS		
I1	13 P	26 P		20 P	18 P	16 P						(456)		PASS
TOT	36 8 A 2 16.0	64 7 B+ 3 21.0	35 8 A 1 8.0	63 5 C 3 15.0	43 4 D 3 12.0	51 5 C 3 15.0	30 7 B+ 1 7.0	27 5 C 1 5.0	49 7 B+ 2 14.0	27 5 C 2 10.0	31 7 B+ 2 14.0	23	137.0	5.95652

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						TOTAL (800)	RESULT	REMARK
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	äC	äCG	äCG
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								

	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C			
	132410018					DHIWAR SIDDHESH RAJENDRA					Regular		MALE			(MU0341120240210529)					MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202																										
T1						16	P				12	P									12	P				12	P				26	P				27	P				28	P			
O1						19	P														16	P				12	P				14	P											
E1	25	P				31	P				33	P				20	*4	P			24	P																				MARKS		
I1	17	P				27	P				19	P				19	P				20	P																				(433)		PASS
TOT	42	9	A+	2	18.0	58	6	B	3	18.0	35	8	A	1	8.0	64	5	C	3	15.0	43	4	D	3	12.0	44	4	D	3	12.0	28	6	B	1	6.0	24	4	D	1	4.0	40	5	C	2	10.0	27	5	C	2	10.0	28	6	B	2	12.0	23	125.0	5.43478

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						TOTAL (800)	RESULT	REMARK
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	äC	äCG	äCG
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								

	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C	TOT	GP	G	C	G*C			
	132410019					EGADE TEJAS SANTOSH					Regular		MALE			(MU0341120252004725)					MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202																										
T1						20	P				18	P									19	P				19	P				42	P				36	P				38	P			
O1						17	P														19	P				15	P				19	P											
E1	21	P				38	P				25	P				35	P				31	P																				MARKS		
I1	12	P				32	P				26	P				25	P				16	P																				(523)		PASS
TOT	33	7	B+	2	14.0	70	8	A	3	24.0	37	8	A	1	8.0	69	6	B	3	18.0	60	7	B+	3	21.0	47	4	D	3	12.0	38	8	A	1	8.0	34	7	B+	1	7.0	61	9	A+	2	18.0	36	8	A	2	16.0	38	8	A	2	16.0	23	162.0	7.04348

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

University Of Mumbai

Sep 01, 2026
Declaration Date:Sep 01, 2026

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO | NAME | STATUS | GENDER | ERN | COLLEGE

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
	132410020	GAIDHANI PARITOSH CHARUDATT		Regular MALE	(MU0341120240210508)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1			22 P	17 P			19 P	17 P	38 P	30 P	32 P			
O1			20 P				20 P	14 P	19 P					
E1	21 P	33 P		33 P	29 P	37 P						MARKS		
I1	15 P	32 P		27 P	24 P	20 P						(519)		PASS
TOT	36 8 A 2 16.0	65 7 B+ 3 21.0	42 9 A+ 1 9.0	77 7 B+ 3 21.0	53 5 C 3 15.0	57 6 B 3 18.0	39 8 A 1 8.0	31 7 B+ 1 7.0	57 8 A 2 16.0	30 7 B+ 2 14.0	32 7 B+ 2 14.0	23	159.0	6.91304

SEAT NO | NAME | STATUS | GENDER | ERN | COLLEGE

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
	132410021	GAJBE KUNAL PRAVIN		Regular MALE	(MU0341120240210503)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1			23 P	23 P			22 P	18 P	38 P	31 P	32 P			
O1			22 P				21 P	12 P	20 P					
E1	27 P	42 P		51 P	37 P	42 P						MARKS		
I1	17 P	35 P		35 P	27 P	23 P						(598)		PASS
TOT	44 9 A+ 2 18.0	77 8 A 3 24.0	45 10 O 1 10.0	109 9 A+ 3 27.0	64 7 B+ 3 21.0	65 7 B+ 3 21.0	43 9 A+ 1 9.0	30 7 B+ 1 7.0	58 8 A 2 16.0	31 7 B+ 2 14.0	32 7 B+ 2 14.0	23	181.0	7.86957

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

PAGE : 13

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

SEAT NO: 132410022 | NAME: HARMALE VEDANT SANDEEP | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240210496) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			18 P	19 P			18 P	16 P	38 P	31 P	35 P			
O1			19 P				21 P	15 P	20 P					
E1	28 P	35 P		32 P	29 P	30 P						MARKS		
I1	16 P	30 P		29 P	29 P	18 P						(526)		PASS
TOT	44 9 A+ 2 18.0	65 7 B+ 3 21.0	37 8 A 1 8.0	80 7 B+ 3 21.0	58 6 B 3 18.0	48 4 D 3 12.0	39 8 A 1 8.0	31 7 B+ 1 7.0	58 8 A 2 16.0	31 7 B+ 2 14.0	35 8 A 2 16.0	23	159.0	6.91304

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

SEAT NO: 132410023 | NAME: JADHAV AAYUSH JAYKUMAR | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240226673) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			16 P	18 P			17 P	16 P	34 P	29 P	34 P			
O1			18 P				19 P	15 P	15 P					
E1	27 P	37 P		39 P	32 P	34 P						MARKS		
I1	12 P	16 P		22 P	17 P	16 P						(483)		PASS
TOT	39 8 A 2 16.0	53 5 C 3 15.0	34 7 B+ 1 7.0	79 7 B+ 3 21.0	49 4 D 3 12.0	50 5 C 3 15.0	36 8 A 1 8.0	31 7 B+ 1 7.0	49 7 B+ 2 14.0	29 6 B 2 12.0	34 7 B+ 2 14.0	23	141.0	6.13043

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

PAGE : 14

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)				
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)						
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)									
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)									
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
132410024	JHA ABHISHEK SANTOSH		Regular	MALE	(MU0341120240210501)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1		22 P	17 P				21 P	17 P	40 P	31 P	30 P				
O1		23 P					22 P	16 P	22 P						
E1 26 P	40 P		39 P		25 P	41 P							MARKS		
I1 10 P	27 P		30 P		29 P	18 P							(546)		PASS
TOT 36 8 A 2 16.0	67 7 B+ 3 21.0	45 10 O 1 10.0	86 7 B+ 3 21.0		54 5 C 3 15.0	59 6 B 3 18.0	43 9 A+ 1 9.0	33 7 B+ 1 7.0	62 9 A+ 2 18.0	31 7 B+ 2 14.0	30 7 B+ 2 14.0		23	163.0	7.08696

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)				
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)						
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)									
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)									
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
132410025	KHAMKAR DEVENDRA UMESH		Regular	MALE	(MU0341120252006267)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1		19 P	18 P				19 P	16 P	38 P	38 P	39 P				
O1		19 P					21 P	18 P	23 P						
E1 22 P	46 P		51 P		47 P	47 P							MARKS		
I1 19 P	29 P		28 P		33 P	26 P							(616)		PASS
TOT 41 9 A+ 2 18.0	75 8 A 3 24.0	38 8 A 1 8.0	97 8 A 3 24.0		80 9 A+ 3 27.0	73 8 A 3 24.0	40 9 A+ 1 9.0	34 7 B+ 1 7.0	61 9 A+ 2 18.0	38 8 A 2 16.0	39 8 A 2 16.0		23	191.0	8.30435

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE
132410026	KHASGIWALA PARAM PAWAN		Regular	MALE	(MU0341120240210489)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			19 P	18 P			17 P	14 P	30 P	34 P	28 P			
O1			20 P				21 P	22 P	18 P					
E1	23 P	43 P		39 P	43 P	34 P						MARKS		
I1	17 P	27 P		27 P	21 P	23 P						(538)		PASS
TOT	40 9 A+ 2 18.0	70 8 A 3 24.0	39 8 A 1 8.0	84 7 B+ 3 21.0	64 7 B+ 3 21.0	57 6 B 3 18.0	38 8 A 1 8.0	36 8 A 1 8.0	48 7 B+ 2 14.0	34 7 B+ 2 14.0	28 6 B 2 12.0	23	166.0	7.21739

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE
132410027	KHATRI ABDUL MATEEN SAJID		Regular	MALE	(MU0341120252004632)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			15 P	12 P			15 P	15 P	28 P	20 P	27 P			
O1			15 P				17 P	12 P	10 P					
E1	23 P	31 P		24 P	25 P	27 P						MARKS		
I1	13 P	18 P		16 P	18 P	16 P						(397)		PASS
TOT	36 8 A 2 16.0	49 4 D 3 12.0	30 7 B+ 1 7.0	52 4 D 3 12.0	43 4 D 3 12.0	43 4 D 3 12.0	32 7 B+ 1 7.0	27 5 C 1 5.0	38 5 C 2 10.0	20 4 D 2 8.0	27 5 C 2 10.0	23	111.0	4.82609

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME		STATUS	GENDER / ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)		
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)	External (60/24) Internal(40/16)							
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		
132410028	KOTHMIRE VAISHNAVI SACHIN		Regular	FEMALE (MU0341120252006083)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1			18 P	15 P			19 P	17 P	34 P	33 P	30 P		
O1			21 P				20 P	18 P	15 P				
E1	23 P	43 P		37 P	32 P	37 P						MARKS	
I1	15 P	26 P		19 P	26 P	17 P						(515)	PASS
TOT	38 8 A 2 16.0	69 7 B+ 3 21.0	39 8 A 1 8.0	71 6 B 3 18.0	58 6 B 3 18.0	54 5 C 3 15.0	39 8 A 1 8.0	35 8 A 1 8.0	49 7 B+ 2 14.0	33 7 B+ 2 14.0	30 7 B+ 2 14.0	23	154.0 6.69565

SEAT NO	NAME		STATUS	GENDER / ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)		
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)	External (60/24) Internal(40/16)							
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		
132410029	KSHIRSAGAR KEDAR BHIMRAO		Regular	MALE (MU0341120240210499)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1			19 P	17 P			17 P	16 P	38 P	37 P	40 P		
O1			19 P				21 P	14 P	20 P				
E1	26 P	42 P		24 P	24 P	36 P						MARKS	
I1	16 P	27 P		21 P	30 P	20 P						(524)	PASS
TOT	42 9 A+ 2 18.0	69 7 B+ 3 21.0	38 8 A 1 8.0	62 4 D 3 12.0	54 5 C 3 15.0	56 6 B 3 18.0	38 8 A 1 8.0	30 7 B+ 1 7.0	58 8 A 2 16.0	37 8 A 2 16.0	40 9 A+ 2 18.0	23	157.0 6.82609

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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	SEAT NO	NAME		STATUS	GENDER ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)		
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)				
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)							
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)							
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		
	132410030	KUDTARKAR TANVI PRADEEP		Regular	FEMALE (MU0341120240210495)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1			22 P	18 P			22 P	18 P	36 P	33 P	37 P		
O1			23 P				22 P	16 P	19 P				
E1	23 P	43 P		43 P	36 P	45 P						MARKS	
I1	19 P	34 P		29 P	30 P	29 P						(597)	PASS
TOT	42 9 A+ 2 18.0	77 8 A 3 24.0	45 10 O 1 10.0	90 8 A 3 24.0	66 7 B+ 3 21.0	74 8 A 3 24.0	44 9 A+ 1 9.0	34 7 B+ 1 7.0	55 8 A 2 16.0	33 7 B+ 2 14.0	37 8 A 2 16.0	23	183.0 7.95652

	SEAT NO	NAME		STATUS	GENDER ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)		
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)				
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)							
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)							
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		
	132410031	KURALE RUCHITA VINOD		Regular	FEMALE (MU0341120240210507)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1			22 P	19 P			19 P	19 P	34 P	33 P	35 P		
O1			23 P				20 P	12 P	19 P				
E1	26 P	29 P		34 P	24 P	30 P						MARKS	
I1	14 P	33 P		37 P	25 P	22 P						(529)	PASS
TOT	40 9 A+ 2 18.0	62 7 B+ 3 21.0	45 10 O 1 10.0	90 8 A 3 24.0	49 4 D 3 12.0	52 5 C 3 15.0	39 8 A 1 8.0	31 7 B+ 1 7.0	53 8 A 2 16.0	33 7 B+ 2 14.0	35 8 A 2 16.0	23	161.0 7.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410032	MAHATO ANTISH SUNIL	Regular	MALE	(MU0341120240210492)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8)	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16)	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16)	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10)	2994511 Business Model Development (TERM WORK) TERM WORK (50/20)	2994512 Design Thinking (TERM WORK) TERM WORK (50/20)	TOTAL (800) äC	RESULT äCG	REMARK äCG
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			15 P	11 P			17 P	14 P	24 P	20 P	30 P			
O1			17 P				18 P	14 P	12 P					
E1	26 P	16 0 F 0.0		4 0 F 0.0	2 0 F 0.0	24 P						MARKS		
I1	6 0 F 0.0	19 P		19 P	4 0 F 0.0	3 0 F 0.0						(315)		FAILED
TOT	32 0 F 2 0.0	35 0 F 3 0.0	32 7 B+ 1 7.0	34 0 F 3 0.0	6 0 F 3 0.0	27 0 F 3 0.0	35 8 A 1 8.0	28 6 B 1 6.0	36 4 D 2 8.0	20 4 D 2 8.0	30 7 B+ 2 14.0	23	51.0	0.00000

SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410033	MAKWANA JAYESH NITINBHAI	Regular	MALE	(MU0341120240210491)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8)	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16)	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16)	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10)	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10)	2994511 Business Model Development (TERM WORK) TERM WORK (50/20)	2994512 Design Thinking (TERM WORK) TERM WORK (50/20)	TOTAL (800) äC	RESULT äCG	REMARK äCG
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			21 P	17 P			17 P	16 P	34 P	25 P	36 P			
O1			21 P				21 P	15 P	15 P					
E1	28 P	34 P		45 P	33 P	24 P						MARKS		
I1	12 P	27 P		27 P	30 P	17 P						(515)		PASS
TOT	40 9 A+ 2 18.0	61 7 B+ 3 21.0	42 9 A+ 1 9.0	89 8 A 3 24.0	63 7 B+ 3 21.0	41 4 D 3 12.0	38 8 A 1 8.0	31 7 B+ 1 7.0	49 7 B+ 2 14.0	25 5 C 2 10.0	36 8 A 2 16.0	23	160.0	6.95652

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

PAGE : 19

SEAT NO: 132410034 | NAME: MAYURI JAGANNATH JAGTAP | STATUS: Regular | GENDER: FEMALE | ERN: (MU0341120252005515) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			16 P	11 P			11 P	16 P	32 P	31 P	32 P			
O1			18 P				17 P	12 P	14 P					
E1	21 P	28 P		24 P	16 0 F 0.0	19 0 F 0.0						MARKS		
I1	12 P	13 0 F 0.0		16 P	16 P	9 0 F 0.0						(384)		FAILED
TOT	33 7 B+ 2 14.0	41 0 F 3 0.0	34 7 B+ 1 7.0	51 4 D 3 12.0	32 0 F 3 0.0	28 0 F 3 0.0	28 6 B 1 6.0	28 6 B 1 6.0	46 7 B+ 2 14.0	31 7 B+ 2 14.0	32 7 B+ 2 14.0	23	87.0	0.00000

SEAT NO: 132410035 | NAME: MISHRA ANSHIKA YAMINIKANT | STATUS: Regular | GENDER: FEMALE | ERN: (MU0341120240210488) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			22 P	17 P			21 P	16 P	38 P	35 P	45 P			
O1			22 P				21 P	24 P	18 P					
E1	29 P	41 P		38 P	42 P	42 P						MARKS		
I1	18 P	35 P		25 P	31 P	25 P						(615 #10)		PASS
TOT	47 #2 10 O 2 20.0	76 #2 8 A 3 24.0	44 #2 10 O 1 10.0	80 #2 7 B+ 3 21.0	73 #2 8 A 3 24.0	67 7 B+ 3 21.0	42 9 A+ 1 9.0	40 9 A+ 1 9.0	56 8 A 2 16.0	35 8 A 2 16.0	45 10 O 2 20.0	23	190.0	8.26087

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

PAGE : 20

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)			
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
132410036	MISHRA NITISH BECHAN		Regular	MALE	(MU0341120240210532)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1		21 P	19 P				21 P	19 P	40 P	34 P	36 P			
O1		21 P					22 P	15 P	22 P					
E1 29 P	51 P		37 P		42 P	47 P						MARKS		
I1 20 P	31 P		36 P		35 P	23 P						(621)		PASS
TOT 49 10 O 2 20.0	82 9 A+ 3 27.0	42 9 A+ 1 9.0	92 8 A 3 24.0		77 8 A 3 24.0	70 8 A 3 24.0	43 9 A+ 1 9.0	34 7 B+ 1 7.0	62 9 A+ 2 18.0	34 7 B+ 2 14.0	36 8 A 2 16.0	23	192.0	8.34783

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)			
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
132410037	MISHRA SAKSHI JAYPRAKASH		Regular	FEMALE	(MU0341120240210521)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1		23 P	19 P				23 P	19 P	36 P	38 P	45 P			
O1		21 P					23 P	17 P	17 P					
E1 29 P	55 P		47 P		45 P	45 P						MARKS		
I1 20 P	36 P		39 P		36 P	33 P						(666)		PASS
TOT 49 10 O 2 20.0	91 10 O 3 30.0	44 9 A+ 1 9.0	105 9 A+ 3 27.0		81 9 A+ 3 27.0	78 8 A 3 24.0	46 10 O 1 10.0	36 8 A 1 8.0	53 8 A 2 16.0	38 8 A 2 16.0	45 10 O 2 20.0	23	207.0	9.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

PAGE : 21

	SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)				TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)				
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)									
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
	132410038	NADAR SHRINI RAJADURAI		Regular	FEMALE	(MU0341120240210515)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202									
T1			23 P	20 P				22 P	19 P	38 P	37 P	45 P				
O1			22 P					23 P	13 P	19 P						
E1	27 P	45 P		40 P		49 P	37 P							MARKS		
I1	19 P	36 P		29 P		37 P	26 P							(626)		PASS
TOT	46 10 O 2 20.0	81 9 A+ 3 27.0	45 10 O 1 10.0	89 8 A 3 24.0		86 9 A+ 3 27.0	63 7 B+ 3 21.0	45 10 O 1 10.0	32 7 B+ 1 7.0	57 8 A 2 16.0	37 8 A 2 16.0	45 10 O 2 20.0	23	198.0	8.60870	

	SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)				TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)				
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)									
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
	132410039	NAGARKAR AYUSH RAJESH		Regular	MALE	(MU0341120240210493)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202									
T1			17 P	17 P				20 P	18 P	34 P	31 P	31 P				
O1			18 P					21 P	14 P	15 P						
E1	23 P	45 P		37 P		24 P	32 P							MARKS		
I1	15 P	23 P		31 P		27 P	23 P							(516)		PASS
TOT	38 8 A 2 16.0	68 7 B+ 3 21.0	35 8 A 1 8.0	85 7 B+ 3 21.0		51 5 C 3 15.0	55 6 B 3 18.0	41 9 A+ 1 9.0	32 7 B+ 1 7.0	49 7 B+ 2 14.0	31 7 B+ 2 14.0	31 7 B+ 2 14.0	23	157.0	6.82609	

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

PAGE : 22

SEAT NO: 132410040 | NAME: NITYA YADAV | STATUS: Regular | GENDER: FEMALE | ERN: (MU0341120252005580) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			17 P	15 P			20 P	17 P	38 P	32 P	31 P			
O1			18 P				19 P	12 P	15 P					
E1	26 P	40 P		29 P	31 P	36 P						MARKS		
I1	15 P	25 P		23 P	24 P	16 P						(499)		PASS
TOT	41 9 A+ 2 18.0	65 7 B+ 3 21.0	35 8 A 1 8.0	67 5 C 3 15.0	55 6 B 3 18.0	52 5 C 3 15.0	39 8 A 1 8.0	29 6 B 1 6.0	53 8 A 2 16.0	32 7 B+ 2 14.0	31 7 B+ 2 14.0	23	153.0	6.65217

SEAT NO: 132410041 | NAME: PANDEY JIGYASHU ANUJ | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240210500) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			22 P	11 P			20 P	16 P	38 P	37 P	42 P			
O1			21 P				22 P	15 P	19 P					
E1	27 P	47 P		45 P	45 P	35 P						MARKS		
I1	19 P	36 P		26 P	30 P	19 P						(602 #10)		PASS
TOT	46 #2 10 O 2 20.0	83 #2 9 A+ 3 27.0	43 #2 10 O 1 10.0	82 #2 7 B+ 3 21.0	75 #2 8 A 3 24.0	54 5 C 3 15.0	42 9 A+ 1 9.0	31 7 B+ 1 7.0	57 8 A 2 16.0	37 8 A 2 16.0	42 9 A+ 2 18.0	23	183.0	7.95652

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME		STATUS / GENDER	ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)		
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)	External (60/24) Internal(40/16)							
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		

132410042 PATEL SHIVANI LALSAHAB Regular FEMALE (MU0341120240210518) MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT
T1			20 P	21 P			19 P	18 P	36 P	38 P	43 P		
O1			20 P				20 P	14 P	17 P				
E1	22 P	39 P		40 P	31 P	36 P						MARKS	
I1	18 P	30 P		36 P	25 P	25 P						(568)	PASS
TOT	40 9 A+ 2 18.0	69 7 B+ 3 21.0	40 9 A+ 1 9.0	97 8 A 3 24.0	56 6 B 3 18.0	61 7 B+ 3 21.0	39 8 A 1 8.0	32 7 B+ 1 7.0	53 8 A 2 16.0	38 8 A 2 16.0	43 9 A+ 2 18.0	23	176.0 7.65217

SEAT NO	NAME		STATUS / GENDER	ERN	COLLEGE							
	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10)			TERM WORK (25/10) ORAL (25/10)	TERM WORK (25/10) ORAL (25/10)	TERM WORK (50/20) ORAL (25/10)	TERM WORK (50/20)	TERM WORK (50/20)		
	External (30/12) Internal(20/8)	External (60/24) Internal(40/16)		External (60/24) Internal(40/16)	External (60/24) Internal(40/16)	External (60/24) Internal(40/16)							
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		

132410043 PATIL ATHARVA PARAG Regular MALE (MU0341120252004709) MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT
T1			17 P	16 P			13 P	13 P	34 P	29 P	27 P		
O1			20 P				17 P	12 P	18 P				
E1	29 P	44 P		27 P	30 P	27 P						MARKS	
I1	13 P	24 P		16 P	21 P	11 0 F 0.0						(458)	FAILED
TOT	42 9 A+ 2 18.0	68 7 B+ 3 21.0	37 8 A 1 8.0	59 4 D 3 12.0	51 5 C 3 15.0	38 0 F 3 0.0	30 7 B+ 1 7.0	25 5 C 1 5.0	52 7 B+ 2 14.0	29 6 B 2 12.0	27 5 C 2 10.0	23	122.0 0.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME			STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)		2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
		TERM WORK (25/10)		TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)				
		ORAL (25/10)						ORAL (25/10)	ORAL (25/10)	ORAL (25/10)						
External (30/12)	External (60/24)			External (60/24)		External (60/24)	External (60/24)									
Internal(20/8)	Internal(40/16)			Internal(40/16)		Internal(40/16)	Internal(40/16)									
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
132410044	PATIL HARSHAD MAHESH			Regular	MALE	(MU0341120240210506)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202									
T1		21 P		22 P				22 P	19 P	36 P	37 P	39 P				
O1		21 P						21 P	16 P	20 P						
E1 24 P	36 P			24 P		32 P	26 P							MARKS		
I1 14 P	27 P			35 P		29 P	22 P							(543)		PASS
TOT 38 8 A 2 16.0	63 7 B+ 3 21.0	42 9 A+ 1 9.0		81 7 B+ 3 21.0		61 7 B+ 3 21.0	48 4 D 3 12.0	43 9 A+ 1 9.0	35 8 A 1 8.0	56 8 A 2 16.0	37 8 A 2 16.0	39 8 A 2 16.0	23	165.0	7.17391	

SEAT NO	NAME			STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)		2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
		TERM WORK (25/10)		TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)				
		ORAL (25/10)						ORAL (25/10)	ORAL (25/10)	ORAL (25/10)						
External (30/12)	External (60/24)			External (60/24)		External (60/24)	External (60/24)									
Internal(20/8)	Internal(40/16)			Internal(40/16)		Internal(40/16)	Internal(40/16)									
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
132410045	PATIL MANASVI SAMADHAN			Regular	FEMALE	(MU0341120240210516)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202									
T1		22 P		21 P				21 P	18 P	34 P	34 P	39 P				
O1		21 P						21 P	20 P	20 P						
E1 27 P	50 P			33 P		44 P	36 P							MARKS		
I1 16 P	31 P			28 P		36 P	27 P							(599)		PASS
TOT 43 9 A+ 2 18.0	81 9 A+ 3 27.0	43 9 A+ 1 9.0		82 7 B+ 3 21.0		80 9 A+ 3 27.0	63 7 B+ 3 21.0	42 9 A+ 1 9.0	38 8 A 1 8.0	54 8 A 2 16.0	34 7 B+ 2 14.0	39 8 A 2 16.0	23	186.0	8.08696	

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410046	PHATAK RIDDHI MANOJ	Regular	FEMALE	(MU0341120240210517)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			22 P	21 P			21 P	17 P	34 P	35 P	41 P			
O1			22 P				22 P	15 P	20 P					
E1	25 P	41 P		40 P	33 P	33 P						MARKS		
I1	19 P	36 P		34 P	33 P	23 P						(587)		PASS
TOT	44 9 A+ 2 18.0	77 8 A 3 24.0	44 9 A+ 1 9.0	95 8 A 3 24.0	66 7 B+ 3 21.0	56 6 B 3 18.0	43 9 A+ 1 9.0	32 7 B+ 1 7.0	54 8 A 2 16.0	35 8 A 2 16.0	41 9 A+ 2 18.0	23	180.0	7.82609

SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410047	POOJA TAMBE	Regular	FEMALE	(MU0341120252005590)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			18 P	15 P			14 P	17 P	38 P	32 P	32 P			
O1			17 P				19 P	13 P	16 P					
E1	22 P	29 P		24 P	24 P	35 P						MARKS		
I1	19 P	26 P		19 P	23 P	17 P						(469)		PASS
TOT	41 9 A+ 2 18.0	55 6 B 3 18.0	35 8 A 1 8.0	58 4 D 3 12.0	47 4 D 3 12.0	52 5 C 3 15.0	33 7 B+ 1 7.0	30 7 B+ 1 7.0	54 8 A 2 16.0	32 7 B+ 2 14.0	32 7 B+ 2 14.0	23	141.0	6.13043

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410048	PRAJAPATI HITESH TIRTHRAJ	Regular	MALE	(MU0341120240210494)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			20 P	20 P			19 P	16 P	32 P	33 P	38 P			
O1			21 P				20 P	22 P	19 P					
E1	27 P	38 P		30 P	29 P	37 P						MARKS		
I1	16 P	31 P		35 P	29 P	22 P						(554)		PASS
TOT	43 9 A+ 2 18.0	69 7 B+ 3 21.0	41 9 A+ 1 9.0	85 7 B+ 3 21.0	58 6 B 3 18.0	59 6 B 3 18.0	39 8 A 1 8.0	38 8 A 1 8.0	51 7 B+ 2 14.0	33 7 B+ 2 14.0	38 8 A 2 16.0	23	165.0	7.17391

SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410049	PREM DAYANAND KADAM	Regular	MALE	(MU0341120252004732)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			18 P	15 P			14 P	17 P	36 P	33 P	32 P			
O1			17 P				20 P	16 P	19 P					
E1	26 P	40 P		24 P	38 P	32 P						MARKS		
I1	13 P	25 P		24 P	22 P	19 P						(500)		PASS
TOT	39 8 A 2 16.0	65 7 B+ 3 21.0	35 8 A 1 8.0	63 5 C 3 15.0	60 7 B+ 3 21.0	51 5 C 3 15.0	34 7 B+ 1 7.0	33 7 B+ 1 7.0	55 8 A 2 16.0	33 7 B+ 2 14.0	32 7 B+ 2 14.0	23	154.0	6.69565

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME		STATUS / GENDER	ERN	COLLEGE								
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

132410050 RAUT SHARVI ANIL Regular FEMALE (MU0341120240210524) MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			19 P	19 P			19 P	17 P	34 P	32 P	33 P			
O1			20 P				20 P	14 P	15 P					
E1	17 P	38 P		24 P	24 P	29 P						MARKS		
I1	14 P	22 P		21 P	26 P	16 P						(473)		PASS
TOT	31 7 B+ 2 14.0	60 7 B+ 3 21.0	39 8 A 1 8.0	64 5 C 3 15.0	50 5 C 3 15.0	45 4 D 3 12.0	39 8 A 1 8.0	31 7 B+ 1 7.0	49 7 B+ 2 14.0	32 7 B+ 2 14.0	33 7 B+ 2 14.0	23	142.0	6.17391

SEAT NO	NAME		STATUS / GENDER	ERN	COLLEGE								
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

132410051 RAUT TANMAY SANDESH Regular MALE (MU0341120240210513) MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			21 P	20 P			21 P	18 P	34 P	32 P	42 P			
O1			21 P				21 P	22 P	17 P					
E1	28 P	49 P		43 P	33 P	31 P						MARKS		
I1	17 P	30 P		37 P	28 P	22 P						(587)		PASS
TOT	45 10 O 2 20.0	79 8 A 3 24.0	42 9 A+ 1 9.0	100 9 A+ 3 27.0	61 7 B+ 3 21.0	53 5 C 3 15.0	42 9 A+ 1 9.0	40 9 A+ 1 9.0	51 7 B+ 2 14.0	32 7 B+ 2 14.0	42 9 A+ 2 18.0	23	180.0	7.82609

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO: 132410052 | NAME: SANSKAR RANE | STATUS: Regular | GENDER: MALE | ERN: (MU0341120252006621) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			20 P	20 P			19 P	17 P	42 P	36 P	43 P			
O1			20 P				20 P	14 P	20 P					
E1	22 P	47 P		24 P	29 P	29 P						MARKS		
I1	11 P	29 P		18 P	20 P	17 P						(517)		PASS
TOT	33 7 B+ 2 14.0	76 8 A 3 24.0	40 9 A+ 1 9.0	62 4 D 3 12.0	49 4 D 3 12.0	46 4 D 3 12.0	39 8 A 1 8.0	31 7 B+ 1 7.0	62 9 A+ 2 18.0	36 8 A 2 16.0	43 9 A+ 2 18.0	23	150.0	6.52174

SEAT NO: 132410053 | NAME: SATYASHEEL AJIT MOHITE | STATUS: Regular | GENDER: MALE | ERN: (MU0341120252006931) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			15 P	11 P			17 P	15 P	22 P	20 P	29 P			
O1			16 P				17 P	12 P	5 0 F 0.0					
E1	16 P	24 P		31 P	24 P	24 P						MARKS		
I1	10 P	10 0 F 0.0		18 P	13 0 F 0.0	10 0 F 0.0						(359)		FAILED
TOT	26 5 C 2 10.0	34 0 F 3 0.0	31 7 B+ 1 7.0	60 4 D 3 12.0	37 0 F 3 0.0	34 0 F 3 0.0	34 7 B+ 1 7.0	27 5 C 1 5.0	27 0 F 2 0.0	20 4 D 2 8.0	29 6 B 2 12.0	23	61.0	0.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)				
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)						
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)									
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)									
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
132410054	SAVLA SOUMYA SHAILESH		Regular	MALE	(MU0341120240210522)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1		19 P	17 P				18 P	14 P	30 P	32 P	38 P				
O1		20 P					19 P	22 P	17 P						
E1 27 P	38 P		24 P		28 P	27 P							MARKS		
I1 16 P	28 P		19 P		24 P	16 P							(493)		PASS
TOT 43 9 A+ 2 18.0	66 7 B+ 3 21.0	39 8 A 1 8.0	60 4 D 3 12.0		52 5 C 3 15.0	43 4 D 3 12.0	37 8 A 1 8.0	36 8 A 1 8.0	47 7 B+ 2 14.0	32 7 B+ 2 14.0	38 8 A 2 16.0		23	146.0	6.34783

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE							TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)				
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)				
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)						
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)									
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)									
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C				
132410055	SHARMA ANKIT JITENDRA		Regular	MALE	(MU0341120240210504)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202								
T1		20 P	19 P				19 P	16 P	40 P	37 P	40 P				
O1		20 P					21 P	24 P	21 P						
E1 27 P	41 P		24 P		28 P	28 P							MARKS		
I1 20 P	29 P		33 P		32 P	18 P							(557)		PASS
TOT 47 10 O 2 20.0	70 8 A 3 24.0	40 9 A+ 1 9.0	76 7 B+ 3 21.0		60 7 B+ 3 21.0	46 4 D 3 12.0	40 9 A+ 1 9.0	40 9 A+ 1 9.0	61 9 A+ 2 18.0	37 8 A 2 16.0	40 9 A+ 2 18.0		23	177.0	7.69565

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO: 132410056 | NAME: SHELKE MAYUR PANDHARINATH | STATUS: Regular | GENDER: MALE | ERN: (MU0341120240210525) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			15 P	15 P			16 P	16 P	30 P	23 P	30 P			
O1			17 P				17 P	12 P	15 P					
E1	22 P	22 0 F 0.0		24 P	5 0 F 0.0	19 0 F 0.0						MARKS		
I1	15 P	13 0 F 0.0		17 P	9 0 F 0.0	5 0 F 0.0						(357)		FAILED
TOT	37 8 A 2 16.0	35 0 F 3 0.0	32 7 B+ 1 7.0	56 4 D 3 12.0	14 0 F 3 0.0	24 0 F 3 0.0	33 7 B+ 1 7.0	28 6 B 1 6.0	45 7 B+ 2 14.0	23 4 D 2 8.0	30 7 B+ 2 14.0	23	84.0	0.00000

SEAT NO: 132410057 | NAME: SHETTY KEERTHI LOKESH | STATUS: Regular | GENDER: FEMALE | ERN: (MU0341120240210519) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			20 P	23 P			16 P	16 P	32 P	32 P	36 P			
O1			20 P				21 P	20 P	16 P					
E1	29 P	52 P		34 P	55 P	43 P						MARKS		
I1	14 P	35 P		34 P	31 P	22 P						(601)		PASS
TOT	43 9 A+ 2 18.0	87 9 A+ 3 27.0	40 9 A+ 1 9.0	91 8 A 3 24.0	86 9 A+ 3 27.0	65 7 B+ 3 21.0	37 8 A 1 8.0	36 8 A 1 8.0	48 7 B+ 2 14.0	32 7 B+ 2 14.0	36 8 A 2 16.0	23	186.0	8.08696

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO | NAME | STATUS | GENDER | ERN | COLLEGE

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

132410058 | SHREYAS VISHAL DARJE | Regular | MALE | (MU0341120252005113) | MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			20 P	11 P			16 P	16 P	34 P	35 P	31 P			
O1			20 P				19 P	17 P	17 P					
E1	23 P	47 P		37 P	39 P	32 P						MARKS		
I1	12 P	32 P		19 P	26 P	20 P						(523)		PASS
TOT	35 8 A 2 16.0	79 8 A 3 24.0	40 9 A+ 1 9.0	67 5 C 3 15.0	65 7 B+ 3 21.0	52 5 C 3 15.0	35 8 A 1 8.0	33 7 B+ 1 7.0	51 7 B+ 2 14.0	35 8 A 2 16.0	31 7 B+ 2 14.0	23	159.0	6.91304

SEAT NO | NAME | STATUS | GENDER | ERN | COLLEGE

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

132410059 | SUMIT SATISH DHANAWADE | Regular | MALE | (MU0341120252005042) | MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			17 P	11 P			13 P	16 P	32 P	32 P	29 P			
O1			19 P				19 P	12 P	15 P					
E1	18 P	39 P		16 0 F 0.0	24 P	25 P						MARKS		
I1	10 P	22 P		9 0 F 0.0	20 P	16 P						(414)		FAILED
TOT	28 6 B 2 12.0	61 7 B+ 3 21.0	36 8 A 1 8.0	36 0 F 3 0.0	44 4 D 3 12.0	41 4 D 3 12.0	32 7 B+ 1 7.0	28 6 B 1 6.0	47 7 B+ 2 14.0	32 7 B+ 2 14.0	29 6 B 2 12.0	23	118.0	0.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO: 132410060 | NAME: SURVASE VAIBHAV DATTATRAY | STATUS: Regular | GENDER: MALE | ERN: (MU0341120252004951) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			18 P	22 P			16 P	18 P	34 P	36 P	31 P			
O1			17 P				19 P	12 P	19 P					
E1	21 P	37 P		28 P	35 P	35 P						MARKS		
I1	14 P	27 P		20 P	26 P	18 P						(503)		PASS
TOT	35 8 A 2 16.0	64 7 B+ 3 21.0	35 8 A 1 8.0	70 6 B 3 18.0	61 7 B+ 3 21.0	53 5 C 3 15.0	35 8 A 1 8.0	30 7 B+ 1 7.0	53 8 A 2 16.0	36 8 A 2 16.0	31 7 B+ 2 14.0	23	160.0	6.95652

SEAT NO: 132410061 | NAME: THAKUR NIVIDA RANJAN | STATUS: Regular | GENDER: FEMALE | ERN: (MU0341120240217762) | COLLEGE: MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY) External (30/12) Internal(20/8) TOT GP G C G*C	2114211 Computer Organization & Architecture (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324111 Mathematics-IV (THEORY) TERM WORK (25/10) External (60/24) Internal(40/16) TOT GP G C G*C	2324112 Electronic circuits & Design (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324113 Physics of Semiconductor devices (THEORY) External (60/24) Internal(40/16) TOT GP G C G*C	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL) TERM WORK (25/10) ORAL (25/10) TOT GP G C G*C	2324413 Creative Coding in Python (TERM WORK AND ORAL) TERM WORK (50/20) ORAL (25/10) TOT GP G C G*C	2994511 Business Model Development (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	2994512 Design Thinking (TERM WORK) TERM WORK (50/20) TOT GP G C G*C	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			22 P	24 P			20 P	16 P	34 P	33 P	45 P			
O1			19 P				22 P	18 P	16 P					
E1	26 P	45 P		34 P	45 P	44 P						MARKS		
I1	16 P	35 P		38 P	35 P	27 P						(614)		PASS
TOT	42 9 A+ 2 18.0	80 9 A+ 3 27.0	41 9 A+ 1 9.0	96 8 A 3 24.0	80 9 A+ 3 27.0	71 8 A 3 24.0	42 9 A+ 1 9.0	34 7 B+ 1 7.0	50 7 B+ 2 14.0	33 7 B+ 2 14.0	45 10 O 2 20.0	23	193.0	8.39130

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE								
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
132410062	THORAT PARAS SANTOSH		Regular	MALE	(MU0341120252005616)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1		17 P	11 P				11 P	15 P	38 P	32 P	30 P			
O1		17 P					19 P	14 P	15 P					
E1 20 P	35 P		14 0 F 0.0		24 P	27 P						MARKS		
I1 11 P	19 P		8 0 F 0.0		16 P	17 P						(410)		FAILED
TOT 31 7 B+ 2 14.0	54 5 C 3 15.0	34 7 B+ 1 7.0	33 0 F 3 0.0		40 4 D 3 12.0	44 4 D 3 12.0	30 7 B+ 1 7.0	29 6 B 1 6.0	53 8 A 2 16.0	32 7 B+ 2 14.0	30 7 B+ 2 14.0	23	117.0	0.00000

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE								
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
132410063	TODARMAL MAYUR UDHAV		Regular	MALE	(MU0341120252005003)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1		17 P	18 P				16 P	16 P	34 P	33 P	30 P			
O1		6 0 F 0.0					19 P	12 P	15 P					
E1 22 P	33 P		24 P		26 P	20 0 F 0.0						MARKS		
I1 12 P	24 P		16 P		19 P	8 0 F 0.0						(420)		FAILED
TOT 34 7 B+ 2 14.0	57 6 B 3 18.0	23 0 F 1 0.0	58 4 D 3 12.0		45 4 D 3 12.0	28 0 F 3 0.0	35 8 A 1 8.0	28 6 B 1 6.0	49 7 B+ 2 14.0	33 7 B+ 2 14.0	30 7 B+ 2 14.0	23	112.0	0.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)		
		ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)				
External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)							
Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)							
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		

132410064 VANMALI SANAL RAJESH Regular MALE (MU0341120240210514) MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			18 P	18 P			17 P	19 P	34 P	25 P	33 P			
O1			21 P				18 P	16 P	17 P					
E1	21 P	27 P		27 P	28 P	24 P						MARKS		
I1	17 P	19 P		21 P	21 P	16 P						(457)		PASS
TOT	38 8 A 2 16.0	46 4 D 3 12.0	39 8 A 1 8.0	66 5 C 3 15.0	49 4 D 3 12.0	40 4 D 3 12.0	35 8 A 1 8.0	35 8 A 1 8.0	51 7 B+ 2 14.0	25 5 C 2 10.0	33 7 B+ 2 14.0	23	129.0	5.60870

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG / REMARK äCG
		TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)		
		ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)				
External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)							
Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)							
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		

132410065 VHATKAR OMKAR RAM Regular MALE (MU0341120240210520) MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL	RESULT	REMARK
T1			20 P	18 P			19 P	16 P	34 P	32 P	39 P			
O1			22 P				21 P	20 P	19 P					
E1	20 P	31 P		24 P	25 P	27 P						MARKS		
I1	16 P	31 P		26 P	23 P	23 P						(506)		PASS
TOT	36 8 A 2 16.0	62 7 B+ 3 21.0	42 9 A+ 1 9.0	68 5 C 3 15.0	48 4 D 3 12.0	50 5 C 3 15.0	40 9 A+ 1 9.0	36 8 A 1 8.0	53 8 A 2 16.0	32 7 B+ 2 14.0	39 8 A 2 16.0	23	151.0	6.56522

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

University Of Mumbai

Sep 01, 2026
Declaration Date:Sep 01, 2026

OFFICE REGISTER FOR THE Bachelor of Engineering(Electronics Engineering (VLSI Design and Technology)) (Semester - IV) (NEP 2020) REGULAR EXAMINATION HELD IN MAY 2026

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SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410066	VIGNESH JAGDISH GHADI	Regular	MALE	(MU0341120252004687)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
T1			18 P	14 P			17 P	18 P	40 P	29 P	40 P			
O1			19 P				18 P	13 P	17 P					
E1	19 P	27 P		28 P	27 P	29 P						MARKS		
I1	13 P	22 P		26 P	22 P	17 P						(473)		PASS
TOT	32 7 B+ 2 14.0	49 4 D 3 12.0	37 8 A 1 8.0	68 5 C 3 15.0	49 4 D 3 12.0	46 4 D 3 12.0	35 8 A 1 8.0	31 7 B+ 1 7.0	57 8 A 2 16.0	29 6 B 2 12.0	40 9 A+ 2 18.0	23	134.0	5.82609

SEAT NO	NAME	STATUS	GENDER	ERN	COLLEGE
132410067	YADAV ANSHU SANJAY	Regular	MALE	(MU0341120240210502)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202

	1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)	2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)	TOTAL (800) äC	RESULT äCG	REMARK äCG
			TERM WORK (25/10)	TERM WORK (25/10)			TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
			ORAL (25/10)				ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
	External (30/12)	External (60/24)		External (60/24)	External (60/24)	External (60/24)								
	Internal(20/8)	Internal(40/16)		Internal(40/16)	Internal(40/16)	Internal(40/16)								
	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			

	1014311	2114211	2114212	2324111	2324112	2324113	2324114	2324115	2324413	2994511	2994512	TOTAL (800) äC	RESULT äCG	REMARK äCG
T1			21 P	23 P			20 P	21 P	34 P	39 P	38 P			
O1			22 P				21 P	13 P	20 P					
E1	25 P	44 P		46 P	43 P	41 P						MARKS		
I1	18 P	32 P		33 P	33 P	18 P						(605)		PASS
TOT	43 9 A+ 2 18.0	76 8 A 3 24.0	43 9 A+ 1 9.0	102 9 A+ 3 27.0	76 8 A 3 24.0	59 6 B 3 18.0	41 9 A+ 1 9.0	34 7 B+ 1 7.0	54 8 A 2 16.0	39 8 A 2 16.0	38 8 A 2 16.0	23	184.0	8.00000

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0

PAGE : 36

SEAT NO	NAME		STATUS	GENDER	ERN	COLLEGE						TOTAL (800) äC	RESULT äCG	REMARK äCG
1014311 Digital Marketing (THEORY)	2114211 Computer Organization & Architecture (THEORY)	2114212 Computer Organization & Architecture Lab (TERM WORK AND ORAL)	2324111 Mathematics-IV (THEORY)		2324112 Electronic circuits & Design (THEORY)	2324113 Physics of Semiconductor devices (THEORY)	2324114 Electronic circuits & Design lab (TERM WORK AND ORAL)	2324115 Physics of Semiconductor devices Lab (TERM WORK AND ORAL)	2324413 Creative Coding in Python (TERM WORK AND ORAL)	2994511 Business Model Development (TERM WORK)	2994512 Design Thinking (TERM WORK)			
		TERM WORK (25/10)	TERM WORK (25/10)				TERM WORK (25/10)	TERM WORK (25/10)	TERM WORK (50/20)	TERM WORK (50/20)	TERM WORK (50/20)			
		ORAL (25/10)					ORAL (25/10)	ORAL (25/10)	ORAL (25/10)					
External (30/12)	External (60/24)		External (60/24)		External (60/24)	External (60/24)								
Internal(20/8)	Internal(40/16)		Internal(40/16)		Internal(40/16)	Internal(40/16)								
TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C		TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C	TOT GP G C G*C			
132410068	YASH		Regular	MALE	(MU0341120252004728)	MU-0466: VIDYAVARDHINIS COLLEGE OF ENGINEERING AND TECHNOLOGY VIDYAVARDHINIS COLLEGE CAMPUS VASAI ROAD (WESTERN RAILWAY) DIST THANE 401 202							
T1		18 P	15 P				16 P	14 P	40 P	34 P	36 P			
O1		18 P					20 P	18 P	17 P					
E1 28 P	50 P		24 P		39 P	33 P						MARKS		
I1 16 P	22 P		21 P		22 P	16 P						(517)		PASS
TOT 44 9 A+ 2 18.0	72 8 A 3 24.0	36 8 A 1 8.0	60 4 D 3 12.0		61 7 B+ 3 21.0	49 4 D 3 12.0	36 8 A 1 8.0	32 7 B+ 1 7.0	57 8 A 2 16.0	34 7 B+ 2 14.0	36 8 A 2 16.0	23	156.0	6.78261

#:0.229; @:O.5042A/O.5043A/O.5044A; *:O.5045A; AA/ABS: ABSENT; P: SUCCESSFUL; F: UNSUCCESSFUL; E: EXMP CAN BE CLAIMED; ~: Dyslexia; +: MARKS CARRIED FORWARD; $: ADDITIONAL CREDIT; RCC: O.5050; RPV: PROVISIONAL; NULL: NULL & VOID.; ADC: ADMISSION CANCELLED; RR: RESERVED; C: CREDIT POINTS EARNED; G: GRADE POINTS; äC: SUM OF C; äCG: SUM OF CxG; SGPI: SEMESTER GRADE PERFORMANCE INDEX = äCG / äC; RR: RESERVED;

(NEP 2020) EXAMINATION HELD IN MAY 2026

%Marks	>=90	>=80 and <90	>=70 and <80	>=60 and <70	>=55 and <60	>=50 and <55	>=40 and <50	< 40
Grade	O	A+	A	B+	B	C	D	F
GRADE POINT	10	9	8	7	6	5	4	0